



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,971	01/29/2004	Yin Yen Bong	2085-01300	4332
23505	7590	11/29/2005	EXAMINER	
CONLEY ROSE, P.C. P. O. BOX 3267 HOUSTON, TX 77253-3267			CHU, CHRIS C	
			ART UNIT	PAPER NUMBER
			2815	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/766,971

Applicant(s)

BONG, YIN YEN

Examiner

Chris C. Chu

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 September 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 - 30 is/are pending in the application.
- 4a) Of the above claim(s) 12 - 14, 17 - 20 and 27 - 30 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 - 11, 15, 16 and 21 - 26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 January 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>5/3/04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on September 6, 2005 has been received and entered in the case.

Election/Restrictions

2. Applicant's election with traverse of Species II in the reply filed on September 6, 2005 is acknowledged. The traversal is on the ground that since applicant provides an allowable generic claim and all other claims are written in dependent form or otherwise include all limitations of the generic claim, the requirement for election is improper. This is not found persuasive because Examiner couldn't find any allowable generic claim or allowable generic limitations in the claims. Since the restriction mailed on July 7, 2005 clearly provides the basis for designating the divided species as patentably distinct, the restriction is still generally deemed to be proper.

The requirement is still deemed proper and is therefore made FINAL.

3. Applicant elected claims: 1 – 11, 15, 16 and 21 – 27. However, a quick review of Fig. 3 shows that the newly amended claim 27 does not read on Species II. Therefore, claims 12 – 14, 17 – 20 and 27 – 30 have been treated as a non-elected Species and are hereby withdrawn from consideration consistent with the election that filed on July 7, 2005 as addressed above.

Art Unit: 2815

(A) In claim 27, the limitation “each of at least a portion of the plurality of pillars being formed abutting at least another one of the plurality of pillars ...” does not read on Fig. 3.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore,

- (A) The combined structure of the following limitation in claim 15 “the first integrated circuit comprising an antenna” with the limitations in claim 1.
- (B) The combined structure of the following limitation in claim 16 “the first electrically conductive pattern being at least a portion of a data transceiver circuit” with the limitations in claim 1.
- (C) The following limitation in claim 26 “a first semiconductor chip having a first integrated circuit, the first integrated circuit comprising an antenna; a substrate having a data transceiver circuit formed thereon”.

must be shown or the features canceled from the claim. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure

Art Unit: 2815

must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

5. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 15, 16 and 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

(A) In claim 15, it is unclear what the applicant regards as “the first integrated circuit comprising an antenna.” That is, the following limitation in claim 1 “a substrate having a first electrically conductive pattern ... being an antenna layer” provides that the substrate has the antenna. Thus, it is unclear that the claimed structure is a stacked antenna chips or an IC chip on an antenna chip/substrate.

(B) In claim 16, it is unclear what the applicant regards as “the first electrically conductive pattern being at least a portion of a data transceiver circuit.” That is, the following limitation in claim 1 “a substrate having a first electrically conductive pattern ... being an antenna layer” provides that the substrate has an antenna. Thus, it is unclear that how could the first electrically conductive pattern be a data transceiver circuit?

(C) In claim 22, line 2, “the antenna pattern” lacks antecedent basis.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

Art Unit: 2815

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1 – 11 and 21 – 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Chung (U. S. Pat. No. 6,421,013).

Regarding claim 1, Chung discloses in e.g., Fig. 6 a structure package (the package in Fig. 6) comprising:

- a first semiconductor chip (40; column 3, lines 56 – 58) having a first integrated circuit (the integrated circuits in the IC chip 40);
- a substrate (20; column 3, line 64) having a first electrically conductive pattern (30B that includes 37b and 38b; see Fig. 5 and column 10, lines 19 – 22) formed thereon, the first electrically conductive pattern (30B that includes 37b and 38b) being an antenna layer (column 10, line 19); and
- a plurality of pillars (42 and 44; column 3, line 58), at least one (42 or 44) of the plurality of pillars (42 and 44) extending from the first semiconductor chip (40) to the substrate (20) for structurally intercoupling and spatially interdisplacing (column 3, lines 62 – 66) the first semiconductor chip (40) and the substrate (20) for forming a first channel (the gap between the chip 40 and the substrate 20) therebetween (see e.g., Fig. 6),
- wherein at least one (42) of the plurality of pillars (42 and 44) is for electrically communicating the first integrated circuit (the integrated circuits in the IC chip 40)

with the first electrically conductive pattern (30B that includes 37b and 38b; see e.g., Fig. 6).

Regarding claim 2, Chung discloses in e.g., Fig. 6 the integrated circuit (the integrated circuits in the IC chip 40) being a data transceiver circuit (abstract, lines 1 – 4 and column 1, lines 11 – 34) in operative communication with the first electrically conductive pattern (30B that includes 37b and 38b; see e.g., Fig. 6).

Regarding claim 3, Chung discloses in e.g., Fig. 6 further comprising:

- a second electrically conductive pattern (30A that includes 37a and 38a; see Fig. 4 and column 10, lines 9 – 15), the first electrically conductive pattern (30B that includes 37b and 38b) and the second electrically conductive pattern (30A that includes 37a and 38a) being formed on two outwardly opposing faces of the substrate (20; see Figs. 4 – 6),
- wherein at least one (44) of the plurality of pillars (42 and 44) is for electrically communicating the integrated circuit (the integrated circuits in the IC chip 40) with the second electrically conductive pattern (30A that includes 37a and 38a; see e.g., Fig. 6).

Regarding claim 4, Chung discloses in e.g., Fig. 6 the second electrically conductive pattern (30A that includes 37a and 38a) being an antenna layer (column 10, line 9) and the integrated circuit (the integrated circuits in the IC chip 40) being in operative communication with the second electrically conductive pattern (30A that includes 37a and 38a; see e.g., Fig. 6).

Regarding claim 5, Chung discloses in e.g., Fig. 6 the first electrically conductive pattern (30B that includes 37b and 38b) and the second electrically conductive pattern (30A that

Art Unit: 2815

includes 37a and 38a) being for transmitting and receiving data signals (abstract, lines 1 – 4 and column 1, lines 11 – 34).

Regarding claim 6, Chung discloses in e.g., Fig. 6 further comprising:

- at least one inter-connector (50; column 10, line 30) formed through the substrate (20) and the first electrically conductive pattern (30B that includes 37b and 38b), the inter-connector (50) for electrically connecting the second electrically conductive pattern (30A that includes 37a and 38a) to one (44) of the plurality of pillars (42 and 44) to thereby electrically inter-communicate the second electrically conductive pattern (30A that includes 37a and 38a) with the integrated circuit (the integrated circuits in the IC chip 40; see e.g., Fig. 6),
- wherein the at least one inter-connector (50, at the center) is one of electrically insulated from (other coils i.e., 38b in Fig. 5) and in electrical communication with (50, at the right-side, the other end of the antenna 30B; see Figs. 5 and 6) the first electrically conductive pattern (30B that includes 37b and 38b; see e.g., Fig. 6).

Regarding claims 7 and 25, Chung discloses in e.g., Fig. 6 the first semiconductor chip (40) and the substrate (20) being arranged in a stacked configuration (see e.g., Fig. 6) for forming the first channel (the gap between the chip 40 and the substrate 20) between the substrate (20) and the first semiconductor chip (40; see e.g., Fig. 6).

Regarding claim 8, Chung discloses in e.g., Fig. 6 the first channel (the gap between the chip 40 and the substrate 20) being filled with a filler material (58; see e.g., Fig. 6 and column 13, lines 7 – 9).

Art Unit: 2815

Regarding claim 9, Chung discloses in e.g., Fig. 6 a portion of the plurality of pillars (42 and 44) being spaced apart along the substrate (20) when being disposed between the substrate (20) and the first semiconductor chip (40; see e.g., Fig. 6).

Regarding claim 10, Chung discloses in e.g., Fig. 6 at least one of the plurality of pillars (42 and 44) being formed from at least two conductive materials (column 5, lines 41 – 43).

Regarding claim 11, Chung discloses in e.g., Fig. 6 one of the at least two conductive material (column 5, lines 41 – 43) being solder material (column 5, lines 49 – 52).

Regarding claim 21, Chung discloses in e.g., Fig. 6 a data transceiver for transceiving data signals (abstract, lines 1 – 4 and column 1, lines 11 – 34) comprising:

- a first semiconductor chip (40) having a data transceiver circuit (the data transceiver circuit in the IC chip 40; abstract, lines 1 – 4 and column 1, lines 11 – 34);
- a substrate (20) having a first antenna pattern (30B that includes 37b and 38b) formed thereon; and
- a plurality of pillars (42 and 44), at least one (42 or 44) of the plurality of pillars (42 and 44) extending from the first semiconductor chip (40) to the substrate (20) for structurally intercoupling and spatially interdisplacing the first semiconductor chip (40) and the substrate (20) for forming a first channel (the gap between the chip 40 and the substrate 20) therebetween (see e.g., Fig. 6),
- wherein at least one of the plurality of pillars (42 and 44) is for electrically connecting and operatively communicating the data transceiver circuit (the data transceiver circuit in the IC chip 40) with the first antenna pattern (30B that includes 37b and 38b).

Regarding claim 22, Chung discloses in e.g., Fig. 6 further comprising:

- a second antenna pattern (30A that includes 37a and 38a), the antenna pattern (30B that includes 37b and 38b) and the second antenna pattern (30A that includes 37a and 38a) being formed on two outwardly opposing faces of the substrate (see e.g., Fig. 6),
- wherein at least one (44) of the plurality of pillars (42 and 44) is for electrically connecting and operatively communicating the data transceiver circuit (the data transceiver circuit in the IC chip 40) with the second antenna pattern (30A that includes 37a and 38a; see e.g., Fig. 6).

Regarding claim 23, Chung discloses in e.g., Fig. 6 the first antenna pattern (30B that includes 37b and 38b) and the second antenna pattern (30A that includes 37a and 38a) being for transmitting and receiving data signals (abstract, lines 1 – 4 and column 1, lines 11 – 34).

Regarding claim 24, Chung discloses in e.g., Fig. 6 further comprising:

- at least one inter-connector (50) formed through the substrate (20) and the first antenna pattern (30B that includes 37b and 38b), the inter-connector (50) for electrically connecting the second antenna pattern (30A that includes 37a and 38a) to one (44) of the plurality of pillars (42 and 44) to thereby electrically inter-communicate the second antenna pattern (30A that includes 37a and 38a) with the data transceiver circuit (the data transceiver circuit in the IC chip 40),
- wherein the at least one inter-connector (50, at the center) is one of electrically insulated from (other coils i.e., 38b in Fig. 5) and in electrical communication with (50, at the right-side, the other end of the antenna 30B; see Figs. 5 and 6) the first antenna pattern (30B that includes 37b and 38b; see e.g., Fig. 6).

Art Unit: 2815

10. Claims 1, 2, 15, 16, 21 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Kuramochi (U. S. Pat. No. 6,634,564).

Regarding claims 1 and 21, Kuramochi discloses in e.g., Fig. 4A and Fig. 6A a structure package (the package in Fig. 6A) comprising:

- a first semiconductor chip (110; column 4, line 67) having a first integrated circuit (the integrated circuits in the chip 110);
- a substrate (120 and 620; column 4, line 65 and column 13, lines 18 – 30) having a first electrically conductive pattern (621; see Fig. 6A and column 13, lines 22 – 23) formed thereon, the first electrically conductive pattern (621) being an antenna layer (column 13, lines 22 and 23); and
- a plurality of pillars (112a and 112b; column 9, line 53), at least one (112a or 112b) of the plurality of pillars (112a and 112b) extending from the first semiconductor chip (110) to the substrate (120 and 620) for structurally intercoupling and spatially interdisplacing (see e.g., Fig. 4A) the first semiconductor chip (110) and the substrate (120 and 620) for forming a first channel (the gap between the chip 110 and the substrate 120 and 620) therebetween (see e.g., Fig. 4A),
- wherein at least one (112a or 112b) of the plurality of pillars (112a and 112b) is for electrically communicating the first integrated circuit (the integrated circuits in the IC chip 110) with the first electrically conductive pattern (621; see e.g., Figs. 4A and 6A and column 13, lines 18 – 46).

Regarding claim 2, Kuramochi discloses in e.g., Fig. 4A and Fig. 6A the integrated circuit (the integrated circuits in the IC chip 110) being a data transceiver circuit (column 5, lines

Art Unit: 2815

26 – 28) in operative communication with the first electrically conductive pattern (621; see e.g., Figs. 4A and 6A).

Regarding claim 15, Kuramochi discloses in e.g., Fig. 4A and Fig. 6A the first integrated circuit (110) comprising an antenna (115; column 5, lines 29 – 32).

Regarding claim 16, Kuramochi discloses in e.g., Fig. 4A and Fig. 6A the first electrically conductive pattern (621) being at least a portion of a data transceiver circuit (since the element 621 is connected to the chip 110 and a communication antenna 632 for receiving and transmitting data, hence a portion of the element 621 reads as a data transceiver circuit).

Regarding claim 26, Kuramochi discloses in e.g., Fig. 4A a data transceiver (104) for transceiving data signals (column 9, lines 29 – 34) comprising:

- a first semiconductor chip (110) having a first integrated circuit (the integrated circuits in the chip 110), the first integrated circuit comprising an antenna (115);
- a substrate (120) having a data transceiver circuit (151; since the element 151 is connected to the chip 110 for receiving and transmitting data, hence the element 151 reads as a data transceiver circuit) formed thereon (see e.g., Fig. 4A); and
- a plurality of pillars (112a and 112b), at least one (112a or 112b) of the plurality of pillars (112a and 112b) extending from the first semiconductor chip (110) to the substrate (120) for structurally intercoupling and spatially interdisplacing the first semiconductor chip (110) and the substrate (120) for forming a first channel (the gap between the chip 110 and the substrate 120) therebetween (see e.g., Fig. 4A),

Art Unit: 2815

- wherein at least one (112a) of the plurality of pillars (112a and 112b) is for electrically communicating the first integrated circuit (the integrated circuits in the chip 110) with the data transceiver circuit (151; see e.g., Fig. 4A).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Vere et al., Berman et al., Shenoy, Takahashi et al., Suzuya and Chung (U. S. Pat. No. 6,353,420) disclose IC chip on an antenna substrate/chip.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>.

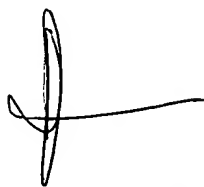
Art Unit: 2815

Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

c.c.

Wednesday, November 23, 2005



SPE Kenneth Parker
Tc2805